IN THE CLAIMS

Please cancel claim 12 without prejudice.

Please substitute the following claims for the pending claims of the same number:

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1. (Amended) A method of preparing a pre-formed integrated circuit chip for encapsulation in an electronic package, comprising the steps of:

forming an interconnect assembly separately from said pre-formed integrated circuit chip;

forming a plurality of conductive bumps connected to the terminals of the pre-formed integrated circuit chip;

bonding said interconnect assembly to said prepared integrated circuit chip;

passivating said bonded interconnect assembly and said pre-formed integrated circuit chip into an integral structure; and

thinning said pre-formed integrated circuit chip to provide said electronic package.

2. (Amended) The method of claim 1 wherein said step of forming said interconnect assembly comprises forming said interconnect assembly on a releasable substrate.

3. (Amended) The method of claim 1 wherein said step of forming said interconnect assembly comprises forming at least one test pad in an interconnect layer,

which at least one test pad can be accessed and electrically connected on opposing sides of said at least one test pad.

4. (Amended) The method of claim 3 wherein said step of forming at least one test pad forms a test pad having gold on a conductive field metal.

5. (Amended) The method of claim 3 wherein said step of forming said interconnect assembly comprises forming at least one test pad in a plurality of stacked interconnect layers, each of which at least one test pad in each interconnect layer can be accessed and electrically connected on opposing sides of said at least one test pad

6. (Amended) The method of claim 5 wherein said step of forming at least one test pad in said plurality of stacked interconnect layers forms at least one test pad in each layer having gold on a conductive field metal.

7. (Amended) The method of claim 1 where said step of forming said plurality of conductive bumps connected to the terminals of the integrated circuit chip forms a metallic bump making connection to a terminal on said integrated circuit chip and a solder layer disposed on said metallic bump.

8. (Amended) The method of claim 7 wherein said step of forming said interconnect assembly comprises forming at least one test pad in an interconnect layer,

which at least one test pad can be accessed and electrically connected on opposing sides of said test pad, and wherein said step of bonding said interconnect assembly to said pre-formed integrated circuit chip flip bonds said solder layer onto one side of said test pad.

9. (Amended) The method of claim 1 where said step of passivating said bonded interconnect assembly and said pre-formed integrated circuit chip into said integral structure to provide said electronic package comprises underfilling said pre-formed integrated circuit chip with an insulating material to remove all voids between said prepared integrated circuit chip and said interconnect assembly.

10. (Amended) The method of claim 1 where said step of passivating said bonded interconnect assembly and said pre-formed integrated circuit chip into said integral structure to provide said electronic package comprises potting said interconnect assembly and said pre-formed integrated circuit chip into an integral package.

11. (Amended) The method of claim 9 where said step of passivating said bonded interconnect assembly and said pre-formed integrated circuit chip into said integral structure to provide said electronic package comprises potting said interconnect assembly and said pre-formed integrated circuit chip into said integral package.

13. (Amended) The method of claim 10 further comprising a step of accessing said pre-formed integrated circuit chip through electrical connection to at least one test pad through a surface thereof opposing said surface of said at least one test pad contacting a terminal of said pre-formed integrated circuit chip to test said pre-formed integrated circuit chip.

14. (Amended) The method of claim 10 and further comprising a plurality of interconnect assembly and pre-formed integrated circuit chips wherein said interconnect assembly and pre-formed integrated circuit chips are bonded together to form a corresponding plurality of electronic packages and further comprising the step of releasing said plurality of electronic packages from each other.

15. (Amended) The method of claim 1 further comprising a plurality of interconnect assembly and pre-formed integrated circuit chips wherein said plurality of interconnect assembly and pre-formed integrated circuit chips are bonded together to form a corresponding plurality of electronic packages and further comprising the step of testing said interconnect assembly and bonding a tested interconnect assembly in said step of bonding said interconnect assembly to said pre-formed integrated circuit chip only if said interconnect assembly tested good.

16. (Amended) The method of claim 15 where said step of forming said plurality of interconnect assemblies comprises forming said interconnect assemblies simultaneously in a wafer and where said plurality of pre-formed integrated circuit chips

are individually bump bonded to successfully tested ones of said interconnect assemblies.

Please add the following claim numbers.

33. A method of preparing a pre-formed integrated circuit chip for encapsulation in an electronic package, comprising the steps of:

forming an interconnect assembly separately from said pre-formed integrated circuit chip, said forming an interconnect assembly including the step of:

forming at least one test pad in a plurality of stacked interconnect layers, each of which at least one test pad in each interconnect layer can be accessed and electrically connected on opposing sides of said at least one test pad.

forming a plurality of conductive bumps connected to the terminals of the pre-formed integrated circuit chip;

bonding said interconnect assembly to said prepared integrated circuit chip; and

passivating said bonded interconnect assembly and said pre-formed integrated circuit chip into an integral structure to provide said electronic package.

34. The method of claim 33 wherein the at least one test pad has gold on a conductive field metal.

35. The method of claim 33 where said step of forming said plurality of conductive bumps connected to the terminals of the integrated circuit chip forms a metallic bump making connection to a terminal on said integrated circuit chip and a solder layer disposed on said metallic bump.

36. The method of claim 35 wherein said step of forming said interconnect assembly comprises forming at least one test pad in an interconnect layer, which at least one test pad can be accessed and electrically connected on opposing sides of said test pad, and wherein said step of bonding said interconnect assembly to said pre-formed integrated circuit chip flip bonds said solder layer onto one side of said test pad.

37. The method of claim 33 where said step of passivating said bonded interconnect assembly and said pre-formed integrated circuit chip into said integral structure to provide said electronic package comprises underfilling said pre-formed integrated circuit chip with an insulating material to remove all voids between said prepared integrated circuit chip and said interconnect assembly.

38. The method of claim 33 where said step of passivating said bonded interconnect assembly and said pre-formed integrated circuit chip into said integral structure to provide said electronic package comprises potting said interconnect assembly and said pre-formed integrated circuit chip into an integral package.

39. The method of claim 37 where said step of passivating said bonded interconnect assembly and said pre-formed integrated circuit chip into said integral structure to provide said electronic package comprises potting said interconnect assembly and said pre-formed integrated circuit chip into said integral package.

40. The method of claim 39 further comprising the step thinning said pre-formed integrated circuit chip.

41. The method of claim 39 further comprising a step of accessing said pre-formed integrated circuit chip through electrical connection to at least one test pad through a surface thereof opposing said surface of said at least one test pad contacting a terminal of said pre-formed integrated circuit chip to test said pre-formed integrated circuit chip.

42. The method of claim 39 and further comprising a plurality of interconnect assembly and pre-formed integrated circuit chips wherein said interconnect assembly and pre-formed integrated circuit chips are bonded together to form a corresponding plurality of electronic packages and further comprising the step of releasing said plurality of electronic packages from each other.

43. The method of claim 39 further comprising a plurality of interconnect assembly and pre-formed integrated circuit chips wherein said plurality of interconnect assembly and pre-formed integrated circuit chips are bonded together to form a corresponding plurality of electronic packages and further comprising the step of testing said interconnect assembly and bonding a tested interconnect assembly in said step of bonding said interconnect assembly to said pre-formed integrated circuit chip only if said interconnect assembly tested good.

44. The method of claim 43 where said step of forming said plurality of interconnect assemblies comprises forming said interconnect assemblies simultaneously in a wafer and where said plurality of pre-formed integrated circuit chips

are individually bump bonded to successfully tested ones of said interconnect assemblies.